IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sun *et al.*	
Serial No.:	10/699,756	Examiner: PATEL, HETUL B
Confirmation No:	4258	Group Art Unit: 2186
Filing Date:	November 3, 2003	
Title:	In-Circuit Configuration Architecture with Configuration on Initialization Function for Embedded Configurable Logic Array	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Pre-Appeal Brief Request for Review

Sir:

Applicants submit this request with the filing of a Notice of Appeal from the decision of the Examiner of Group Art Unit 2186 dated October 1, 2008, rejecting all pending claims 18-30.

Claims 18-30 are rejected under 35 U.S.C. § 102(a) as being anticipated by Sun *et al.* (US 6,401,221; hereinafter "Sun") (see paragraphs 5-6 at pages 3-8 of the Office Action). Applicants respectfully submit that Claims 18-30 are patentable over Sun at least on the grounds as follows.

1.

With respect to one aspect of the claimed invention, the Examiner asserts that Sun discloses the claimed "**configurable logic array**" by equating the claimed configurable logic array with the programmable flash memory of Sun. The Examiner equates the term "configurable" (in the context of the "configurable logic array") with another term "programmable" (in the context of the "programmable flash memory") by merely saying "programmable (i.e. configurable)" without any basis of substantive fact (see particularly the last paragraph starting with "[w]ith respect to (a)" on page 7 of the Office Action).

Applicants respectfully submit that there is clear legal deficiency in the rejection. The relevant patent authorities unambiguously dictate that each claim term be interpreted consistent with its ordinary and customary meaning to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, *>415 F.3d 1303, 1313<, 75 USPQ2d 1321>, 1326< (Fed. Cir. 2005) (*en banc*) ("[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application."). See also MPEP § 2111.01 (III). In the present case, a person of ordinary skill in the art would interpret the technical and **ordinary meaning** of a "configurable logic array" to be quite contrary to, or at least not necessarily related to, the technical and ordinary meaning of a programmable flash memory.

Specifically, the configurable logic array (CLA) was first introduced by S. E. Wahlstrom, entitled "Programmable Logic Arrays--Cheaper by the Millions," Electronics, Dec. 11, 1967, pp. 90-95. In the CLA structure, the interconnections among the internal logic cells or blocks are configurable, even after the CLA device leaves the factory, such that the internal logic cells/blocks can be variably re-interconnected according to supplied configuration data. To the contrary, in a flash memory, the interconnections among the internal cells are fixed after the flash memory leaves the factory. Under the flash memory structure, the contents of the cells of the flash memory are accessed according to applied addresses.

Although the Examiner is permitted to broadly interpret a claim term, the claim term shall not be interpreted so broad as to give a meaning that adversely contradicts the term's ordinary and customary meaning to a person of ordinary skill in the art. In the present case, as discussed above, it is believed that the Examiner's allegation impermissibly runs in direct contradiction with this clear canon of claim construction.

2.

Applicants respectfully submit that there is glaring factual deficiency in the rejection. To the extent Sun does disclose a "programmable flash memory" (cf. col. 4, lines 31-35), the term "programmable" in the context of such a programmable flash memory, in fact, has nothing to do with the term "configurable" in the "configurable logic array." In typical glossaries of flash memory technology, the term "**program**" is related to the specific way of writing data into the cells of a flash memory, rather than to changing the interconnections among its internal cells.

3.

Another reason indicative of the Examiner's improper equating of the "configurable logic array" with the "programmable flash memory" is that the term "configurable logic array" or its acronym "CLA" has, in fact, become a **proper name** in the electronic industry for denoting a group of electronic devices, the internal cells/blocks of which can be configured or variably re-interconnected. It is thus nonsensical for the Examiner to misinterpret the term "configurable" of the **proper name** "configurable logic array" and then to compare/liken it with a "programmable flash memory," not to mention that the term "programmable" itself carries a distinct and different meaning in the context of a "programmable flash memory."

4.

With respect to another aspect of the claimed invention (for example, as stated in Claim 20), the Examiner asserts that Sun discloses the "**configuration data**" by equating the claimed "configurable data" with the "instructions" of Sun. The Examiner seeks to rationalize this assertion by simply saying that "instructions are configurable" (see particularly the second paragraph starting with "[w]ith respect to (b)" on page 8 of the Office Action).

Applicants respectfully traverse the rejection for the following reasons.

Sun does not disclose the claimed configurable logic array as discussed above. Applicants respectfully note that, as a consequence, Sun does not have any "configuration data" stored within a non-existent "configurable logic array."

Moreover, the Examiner's assertion that "instructions are configurable" falls short of providing any adequate or even plausible basis. It is respectfully submitted that, even if "instructions are configurable" as broadly asserted by the Examiner was a relevant statement, the claimed configurable "data" are still not equivalent to configurable "instructions," for the reason that **data** are distinct from **instructions** to a person of ordinary skill in the art. Some reasons are detailed in a previous response to the Office Action dated June 26, 2008, and the reasons are thus omitted here for the sake of brevity (see the second and third paragraphs of section II in that response).

5.

Due to the substantial and substantive differences between the claimed "**configurable logic array**" and the Examiner's asserted "programmable flash memory" of Sun (as discussed in sections 1-3 above), and between the claimed "**configurable data**" and the Examiner's asserted "instructions" of Sun (as discussed in section 4 above), Applicants ardently submit that the Examiner has not provided a sufficient reason in the Office Action for rejecting the claimed invention with respect to the claimed aspects as discussed above, and has not presented a prima facie case of unpatentability as required by the relevant patent authorities. It is well established in patent law that the Examiner bears the burden of presenting a prima facie case of unpatentability. Specifically, the initial burden of making out a prima facie case is on the Examiner. When the Examiner has made out a prima facie case, the burden would then shift to the Applicant to rebut it. On the other hand, if the Examiner at the initial stage does not produce a prima facie case, then the rejection is improper and the Applicant is entitled to grant of the patent. However, in the present case, Applicants believe that the burden of establishing a prima facie case has not been met by the Examiner. This is apparently true as throughout the Office Action, no sufficient reason is furnished by the Examiner to support the asserted rejection.

For the foregoing reasons, Claims 18-30 are believed to be allowable over the cited prior art reference.

Conclusion

In light of the above reasons, Applicants respectfully submit that Claims 18-30 are patentable because:

1. The Examiner has impermissibly interpreted the claimed "configurable logic array" in a way contrary to its ordinary meaning;

2. The Examiner has erroneously interpreted the term "programmable" in the context of the claimed "programmable flash memory";

3. The Examiner has impermissibly interpreted the proper name "configurable logic array;"

4. The Examiner has mistakenly sought to equate Sun's "instructions" with the claimed "data"; and

5. The Examiner has not presented a prima facie case of unpatentability as required by the Patent Law.

To the extent that one or more of the statements submitted above are agreed, it is respectfully submitted that all pending claims should be allowed. Accordingly, the reversal of Examiner's rejection is respectfully solicited.

Should the Examiner believe that a telephone conference with Applicants' representative would be helpful to advance the prosecution of the application, or for any other reason, he or she is kindly invited to contact the undersigned with any questions. The Commissioner is hereby authorized to charge any needed fees to Deposit Account 50-1600.

Respectfully submitted,

Dated: December 17, 2008

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